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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,925	01/09/2006	Peter Bode	853563.428USPC	3791

38106 7590 05/27/2009
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EXAMINER	
GILES, EBONI N	
ART UNIT	**PAPER NUMBER**
2611	
MAIL DATE	**DELIVERY MODE**
05/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/563,925	Applicant(s) BODE, PETER
	Examiner EBONI GILES	**Art Unit** 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This office action is in response to communication filed on 3/9/09. Claims 1-12 are pending in this application of which Claims 2, 8 and 10 are cancelled and Claims 11 and 12 are new.

2. Applicant's arguments with respect to claims 1, 3, 4-7, 9, 11 and 12 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-7, 9, 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,350,950 to Waldmann et al. ("Waldmann) in view of U.S. Patent Pub 2003/00117181 to Powell et al. ("Powell") in further view of U.S. Patent 7,130,368 to Aweya et al ("Aweya").

Regarding Claim 1, Waldmann's first embodiment teaches an "electronic circuit for determining a ratio of a first frequency of a first signal and a second frequency of a second signal," where a circuit arrangement for measuring a frequency is produced which is placed into a fixed relationship with the frequency to be measured, whereby the frequency to be measured and the reference frequency are each supplied to a respective counter (Col. 1, lines 6-12) and

further teaches that the measuring frequency is supplied to a period counter and the reference frequency is supplied to a time counter (Col. 2, lines 16-18, Figure 1, elements B, C,12 and 13). The measuring frequency and reference frequency reading on claimed first and second frequencies of first and second signals;

Waldmann's first embodiment further teaches "a sampling means for sampling first intermediate count values of the first counter when the second counter reaches preset second intermediate count values such that the first counter is sampled under the control of the second counter," where the measuring frequency is measured in a shortest measuring time duration or time slot. A signal at the time TN for the beginning of a measuring period sets the synchronizing flip-flop. The next negative zero passage of the measuring frequency resets this flip-flop. The resetting is delayed until the reference frequency or time counter has stepped through and now causes the storing of the count results of the reference frequency or time counter (Col. 2, lines 40-48). The first counter (timer counter) is synchronized based on the measuring frequency output at the period counter [second counter], once the measuring frequency reaches a falling edge, the timer counter can then proceed with acquiring intermediate count values from the reference frequency;

Waldmann's first embodiment further teaches that "the first and second intermediate count values form a plurality of pairs of intermediate count values of the first and second counters," where the pulse train (B) designates the pulses of the measuring frequency and the pulse train (C) designates the pulses of the

reference frequency of the oscillator (Col. 2, lines 34-37, Figure 1, elements B and C) while further disclosing several successive and stored count results of the reference frequency counter which corresponds to a time measurement, and from several successive and stored count results of the counter for the frequency to be measured (Col. 1, lines 57-61);

Waldmann's first embodiment further discloses "a calculation unit for determining the ratio of the first and second frequencies on the basis of the plurality of pairs of intermediate count values; wherein more than two pairs of intermediate count values are used by the calculation unit for determining the ratio of the first and second frequencies," where the difference between two successive count results of the period counter corresponds to the number of periods during one measuring time duration. The difference of the corresponding count results of the reference frequency or time counter corresponds to the time duration of this measuring time with the resolution of the reference frequency. The microprocessor calculates the quotient from the measured time and from the number of periods counted. The quotient corresponds to the precise period duration or to the frequency which is to be measured (Col. 2, lines 56-66, Figure 1, elements 12, 13 and 16) and further teaches that frequency or period duration for periods of different lengths is computed...from several successive and stored count results of the reference frequency counter (time counter)...and from several successive and stored count results of the counter for the frequency to

be measured (period counter) (Col. 1, lines 55-61) where more than two pairs of the time count and period count are calculated over a pulse train.

Waldmann does not expressly disclose that during the sampling of the first intermediate count value, the first and second counters continue counting.

Powell does expressly teach that "during the sampling of the first intermediate count value, the first and second counters continue counting," where the pulse frequency generally comprises a frequency of an input pulse signal, such that the pulse frequency is determined based on accuracy dependent only upon a reference timer clock. The frequency input signal is generally utilized as a clock for a pulse counter and as a capture latch signal for the system free running timer (¶ 0020).

At the time of the invention, it would have been obvious to a person of ordinary skill to combine an electronic circuit of Waldmann with counters comprising a free running timer of Powell. The free running counters are easily implemented in a fixed time data acquisition period. The reference clock and pulse counters do not require start and stop signals (Powell, ¶ 0088).

Waldmann and Powell do not expressly disclose wherein the ratio of the first and second frequencies is calculated based at least on a regression from pairs of intermediate count values corresponding to different numbers of samples.

Aweya teaches a phase-locked loop (PLL) for synchronizing a local clock to a reference clock. The PLL comprises an oscillator to output a local frequency

and a loop filter for a sequence of time references within a reference clock. An estimate is derived based on the difference between the time reference and local clock time based on a linear trend model of at least one previous estimate (Col. 2, lines 52-63). Using a linear regression analysis, the frequency offset between transmitter and receiver clocks for a given time period is estimated (Col. 1, lines 54-57).

At the time of the invention, it would have been obvious to a person of ordinary skill to combine an electronic circuit of Waldmann and Powell with linear regression analysis of Aweya. The suggestion/motivation would have been in order to provide clock synchronization using linear modeling (Col. 1, lines 52-53).

Regarding Claim 3, Waldmann and Powell disclose an electronic circuit for determining a ratio of a first frequency of a first signal and a second frequency of a second signal as recited in Claim 1.

Waldmann does not expressly disclose a first counter triggered by an edge of a first signal, wherein the second counter is triggered by an edge of a second signal, wherein a clock signal of the second counter is one of first and second signals and wherein the second intermediate count values of the second counter at which the first counter is sampled are preset in a register.

Powell does expressly disclose a timer that is initiated by an enable signal that is triggered at the rising edge of an input pulse. A counter can then be used to count a particular number of pulses. After a predetermined number of pulses have been counted, a trigger generated by the rising edge of the next input signal

disables the timer. The timing diagram indicates that the timing measurement takes place for a fixed number of pulses (¶ 0006, Figure 2). The clock signal is generated based on the input pulse thereby the pulse count is fixed and sampled based on the output of the timer counter (i.e. clock).

At the time of the invention, it would have been obvious to a person of ordinary skill to modify an electronic circuit of Waldmann with counters triggered by edges of their respective signals of Powell. The suggestion/motivation would have been in order to synchronize the pulse count based on a clock signal generated by one of a first or second signal.

Regarding Claim 4, Waldmann and Powell disclose an electronic circuit for determining a ratio of a first frequency of a first signal and a second frequency of a second signal as recited in Claim 1.

Waldmann discloses "a memory comprising a first and second storage," where a memory is connected to the output of a period counter and a memory is connected to the output of the reference frequency or time counter (Col. 2, lines 18-21, Figure 1, elements 12-15);

Waldmann further discloses "the first storage is for storing the first intermediate count values of the first counter such that a sequence of first intermediate count values of the first counter is provided," where a pulse of the frequency to be measured at the end of a measuring period whereby, said control signal controls the storing, or reading-in, of the time count result of the reference frequency into said reference time memory, that a period counter for

the frequency to be measured is triggered by the zero passages (Col. 1, lines 44-48).

Waldmann further discloses “the second storage is for storing the second intermediate count values of the second counter such that a sequence of second intermediate count values of the second counter is provided," where the pulses of the frequency to be measured, that the count result of the period counter for the frequency to be measured is stored in a respective period memory in response to said control signal at the end of a measuring period (Col. 1, lines 51-55).

Regarding Claim 5, Waldmann and Powell disclose an electronic circuit for determining a ratio of a first frequency of a first signal and a second frequency of a second signal as recited in Claim 1.

Powell discloses that "the calculation unit is implemented by a processor, wherein the plurality of pairs of intermediate count values are stored in a working memory of the processor and wherein the working memory is accessed for one of reading and writing of the plurality of pairs of intermediate count values by interrupt routines,” where the first integrated circuit counter generally provides a signal to a comparator and a timer latch. A micro controller [processor] contains a time interrupt line, a write line, a read line, a data bus, and a pulse overflow interrupt line. Micro controller is generally connected to comparator at write line, read line, and time interrupt line. Micro controller is also connected to timer latch and data bus. Additionally, a second integrated circuit counter can provide a first output signal along a line to read line of micro controller. Read line is generally

connected at least one output line of timer latch at node B. Output line is thus tied to read line at node A and node B. Note that node A and node B are essentially the same node. A second output signal of the second integrated circuit counter can be provided to pulse overflow interrupt line of micro controller. The micro controller additionally comprises a first storage register for storing a high order time count and a second storage register for storing a high order pulse count. The second output signal of second integrated circuit counter generally comprises an overflow signal (¶0039-40, Figure 4, elements 46, 48, 50-54, 57, 59-60, 62).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine an electronic circuit of Waldmann with a calculation unit implemented by a processor of Powell. The suggestion/motivation would have been in order to perform a higher order count and automatically measure pulse frequency. A load signal is not required to preload data into the counter and does not require the use of a predetermined pulse count for the measurement of the measurement period thereby taking advantage of commercially available microprocessors (Powell, ¶ 0090).

As to Claim 6, Waldmann and Powell disclose an electronic circuit for determining a ratio of a first frequency of a first signal and a second frequency of a second signal as recited in Claim 1.

Waldmann does not expressly disclose that the calculation unit determines a variation of the frequency ratio over the time.

Powell discloses that “the calculation unit determines a variation of the frequency ratio over the time," where the measurement process begins by reading the current time (counter value) and adding the equivalent of 10 milliseconds in counts and writing this value to a compare register (i.e., comparator). A compare interrupt (i.e., via time interrupt line is then enabled, such that the 16-bit compare interrupt of comparator will generate an interrupt after 10 milliseconds. When the interrupt occurs, an additional 10 milliseconds worth of counts is added to the previous compare value to generate an interrupt 10 milliseconds later. This provides a periodic 10-millisecond interrupt that can be utilized as the time base (¶0042, Figure 4).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine an electronic circuit of Waldmann with a calculation unit of Powell. The suggestion/motivation would have been in order to utilize the last captured pulse count and timer count values (Powell, ¶ 0090).

Method claim 7 is drawn to the method of using the corresponding apparatus claimed in claim 1. Therefore, method claim 7 corresponds to apparatus claim 1 and is rejected for the same reasons of obviousness as used above.

Regarding Claim 9, Waldmann discloses a computer program product in the form of a conventional mini computer that may be used as the microprocessor to perform the functions of the electronic circuit (Col. 4, lines 13-

15) recited in Claim 1 which have limitations similar to those presently treated and are met by the references as discussed above.

Claims 11 and 12 have limitations similar to those treated in the above rejection to Claims 3 and 4 and are met by the references as discussed above.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EBONI GILES whose telephone number is (571)270-7453. The examiner can normally be reached on 7:30 AM - 5 PM, M-F, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ EBONI GILES/
Examiner, Art Unit 2611

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